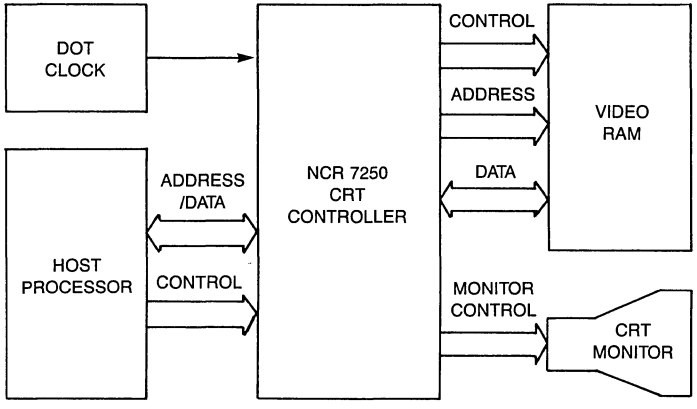
7250
CRT CONTROLLER

- Generates VSYNC, HSYNC, and VIDEO to directly interface with a CRT Monitor
- Eight Screen Functions:
  - —Lines per Page
  - —Screen Blank
  - —Screen Reverse-Video
  - —Video Chop
  - —Split-Screen
  - —Graphics Style
  - —Blank Cursor
  - —Timing Format
- Six Field Functions:
  - —Reverse Video
  - —Highlight
  - —Field Blink
  - —Field Blank
  - —Underline
  - —Graphics Mode
- On-chip character generator (mask programmable) 192 characters standard, up to 256 optional.
- Directly addresses a 2K × 8 Video RAM (VRAM)
- Cursor-address under CPU Control
- Hardware Scrolling for full page or split-screen viewing
- Transparent Refresh for RAM updates at DMA speeds
- Two Timing Formats (including interlace) are available
- Accepts Dot-Clocks up to 20 MHz
- TTL-Compatible signal pins
- Single +5V Power Supply

The NCR 7250 CRT Controller (CRTC) incorporates character generation, video attributes, video timing, RAM interface, and control functions on a single chip. The 7250 provides HSYNC, VSYNC, VIDEO, and HIGHLIGHT (intensity) outputs to directly interface with a raster scan CRT monitor. The character generator produces up to 256 8x12 characters, providing character clarity and variety previously not available in single chip CRT controllers. Features include eight Screen Functions, six Field Functions, hardware scrolling, hardware cursor, and two user-selectable timing formats. The 7250's direct video RAM (VRAM) addressing and transparent refresh permit asynchronous data transfers at DMA speeds without cycle stealing or processor interrupts.

CRTC SYSTEM ENVIRONMENT



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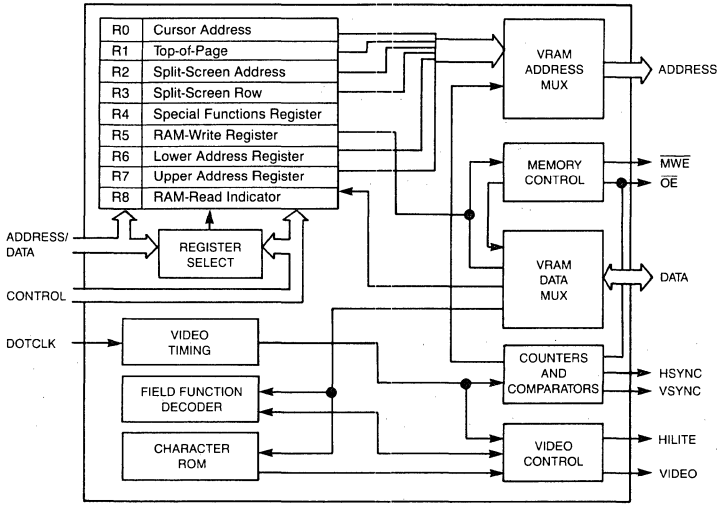
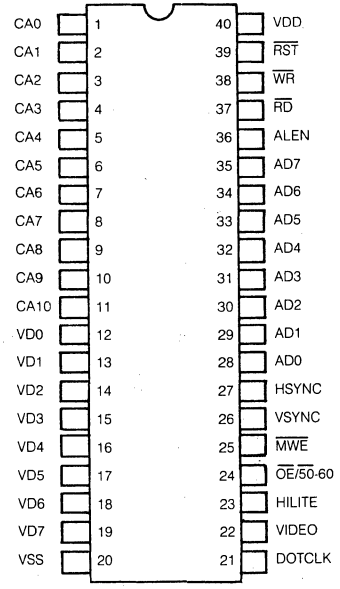
NCR 7250 CRTC ARCHITECTURE

The architecture of the NCR 7250 includes nine software-display control registers, an Address/Data Bus, a VRAM data bus, a VRAM address bus (referred to as the Screen Address Bus), as well as a Character-ROM which holds patterns for 192 characters standard, up to 256 optional.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



CENTRAL PROCESSING UNIT (CPU) INTERFACE

The CPU interface is composed of an 8-bit Address/Data bus (AD0-AD7), nine software display control registers, and three bus control lines ($\overline{RD}$, $\overline{WR}$, ALEN).

At the heart of the CPU interface are the nine software display control registers. These registers enable the CPU to write/read data to the VRAM, position the cursor, vary the size of the split-screen, or select any of the special Screen Functions.

The 8-bit multiplexed Address/Data bus and the three bus controls lines are used by the CPU to designate which of the nine software display control registers is selected. The CPU generates $\overline{RD}$ and $\overline{WR}$ to tell the CRTC that a CPU read or write is occurring. The falling edge of ALEN is used by the CRTC to latch the register address from the address bus. When ALEN is at a low level, the CPU accesses the addressed register. The ability to select the addresses of the display control registers is a mask option.

PIN DESCRIPTION

Pin Name	Pin #	I/O	Description
AD0	28	I/O	Address/Data Bus—Bidirectional bus for interfacing to a multiplexed Address/Data Bus. Used to program internal registers and transfer data to and from the Video RAM.
AD1	29		
AD2	30		
AD3	31		
AD4	32		
AD5	33		
AD6	34		
AD7	35		
$\overline{RD}$	37	I	Bus Read—Control signal generated by the microprocessor. Indicates a CPU read in progress.
$\overline{WR}$	38	I	Bus Write—Control signal generated by the microprocessor. Indicates a CPU write in progress.
$\overline{RST}$	39	I	Reset—Control signal which resets all registers to their default conditions, holds VIDEO to logic 0, but does not affect the generation of VSYNC or HSYNC.
ALEN	36	I	Address Latch Enable—Control Signal, the falling edge of which latches the register addresses from the Address Bus into the CRT. A low level allows CPU access to the CRTC internal registers.
VIDEO	22	O	Video—Contains the DOT stream for the selected row of alphanumeric characters. This DOT stream is modified by various logic conditions (screen and field functions, blank states) which are activated internally by the CRTC.
HILITE	23	O	Highlight Intensity—Used with external circuitry to generate an alternate video intensity level.
VSYNC	26	O	Vertical Sync—Initiates Vertical retrace in the CRT monitor.
HSYNC	27	O	Horizontal Sync—Initiates Horizontal retrace in the CRT monitor.
VD0	12	I/O	RAM Data Bus—Bidirectional bus upon which data is transferred to and from Video RAM. The data represent alphanumeric characters intended for display on the monitor screen, and Special Field Functions which modify the appearance of the characters which follow.
VD1	13		
VD2	14		
VD3	15		
VD4	16		
VD5	17		
VD6	18		
VD7	19		
CA0	1	O	RAM Address Bus—Addresses the Video RAM. (Referred to as the Screen Address Bus.)
CA1	2		
CA2	3		
CA3	4		
CA4	5		
CA5	6		
CA6	7		
CA7	8		
CA8	9		
CA9	10		
CA10	11		
$\overline{MWE}$	25	O	Write Enable—Control signal which tells the VRAM if a write (low level) or a read (high level) is to be executed.
DOTCLK	21	I	Dot Clock—Generated by an external oscillator circuit whose frequency corresponds to the Video Dot Rate. It is asynchronous with the microprocessor interface signals. All other timing signals are derived from this input.
$\overline{OE}/\overline{50}$-60	24	I/O	When $\overline{RST}$ is active, this pin is an input which tells the CRTC which of the two vertical timing counts to use. If $\overline{RST}$ is inactive, this pin is an output for enabling the Video RAM.
VDD	40		Power Supply— + 5 VDC, most positive voltage connection.
VSS	20		Power Supply—0 VDC logic ground, most negative connection.

SOFTWARE DISPLAY CONTROL REGISTERS

The nine software display control registers of the NCR 7250 are addressable by the system and their addresses are selected by the user. Eight of the registers, (R0 through R7) are write-only, while R8 is read-only. The RESET default value of each register is all zeros. This state is assumed after $\overline{RST}$ goes low.

Because R0, R1, and R2 are 11 bits in length, they cannot be loaded directly from the CPU bus. The Screen Address Registers, R6 and R7, are dual purpose registers. They are used as temporary storage registers when R0, R1, or R2 is loaded and contain the VRAM address during VRAM read and write operations. To load an 11 bit register, the 8 lower bits are loaded into R6 and the three upper bits are loaded into R7. The destination register (R0, R1, or R2) is then addressed and a WR command is issued. This WR command causes the value in R6 and R7 to be transferred to the destination register. The data on the CPU bus at the time of this WR command is not used.

CURSOR ADDRESS REGISTER (R0)

The cursor is positioned by writing the desired address to R0 which is an 11-bit register.

TOP-OF-PAGE REGISTER (R1)

This 11-bit register contains the VRAM address of the character that begins the page in the top left corner of the CRT monitor.

SPLIT-SCREEN (SS) ADDRESS REGISTER (R2)

R2 contains the 11-bit VRAM address of the character which begins the designated screen address row.

SPLIT-SCREEN (SS) ROW REGISTER (R3)

The 6-bit SS Row Register contains the value of the row at which the split-screen address is first accessed.

SPECIAL FUNCTIONS REGISTER (R4)

R4 is an 8-bit register that provides CPU control of the eight Screen Functions.

RAM-WRITE REGISTER (R5)

R5 is an 8-bit register used to transfer data bytes from the CPU to VRAM. The screen address (contents of R6 and R7) increments by one after each VRAM write.

LOWER-SCREEN ADDRESS REGISTER (R6)

This 8-bit register comprises the lower 8-bits of the 11-bit Screen Address Bus. This bus addresses VRAM for CPU transfers. R6 is also used in conjunction with R7 to load Registers R0, R1 and R2.

UPPER-SCREEN ADDRESS REGISTER (R7)

R7 is a 3-bit register containing the upper 3-bits of the 11-bit Screen Address Bus. This bus addresses VRAM for CPU transfers. R7 is also used in conjunction with R6 to load Registers R0, R1 and R2.

RAM-READ REGISTER (R8)

The 8-bit RAM-Read Register is used to transfer data bytes from VRAM back to the CPU. The screen address (contents of R6 and R7) increments by one after each VRAM read.

MEMORY

The NCR 7250 CRTC memory information includes the Video RAM interface and the on-chip Character-ROM.

VIDEO RAM INTERFACE

The NCR 7250-VRAM interface is comprised of the Screen Address Bus (CA0-CA10), the VRAM Data Bus (VD0-VD7), and control signals MWE and OE/50-60. The VRAM is a generic 120ns static 2K x 8 RAM used to store display information. The 7250 incorporates a double speed memory technique which permits a refresh access and a CPU access to occur during the time required to display one character. When CPU data is not being written, the CPU access time is used to update the VRAM read register R8 using the VRAM location specified by R6 and R7. If R8 is addressed by the CPU and a RD command issued, the value of R8 will be transferred onto the AD bus and be valid within 120ns. In writing CPU data, CPU data transfers to R5 (RAM Write Register) are asynchronous with respect to VRAM accesses. In order to resolve the possibility of invalid data transfer if a VRAM write is initiated at the end of a VRAM access time, two access times are reserved for the write operation and data is written at both times. At the end of the second VRAM access, indicated by the second pulse edge of $\overline{MWE}$, the Screen Address Register (R6 and R7) increments to the next VRAM location. In order to allow sufficient time for the VRAM write process to occur, a period of 24 t_{cyc} (dot-clks) is required between CPU WR commands. This translates into data transfer rates in excess of 500K bytes/sec for VRAM when using a standard dot-clk frequency of 17.6MHz.

CHARACTER-READ ONLY MEMORY (CHARACTER-ROM)

The on-chip Character-ROM contains dot patterns to generate text, holding patterns for up to 256 alphanumerics. A standard 192 character set is provided in the ROM of each NCR 7250 CRTC. Mask options available for customized character sets are covered under Character Set Options.

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EXTERNAL CLOCK (DOTCLK)

DOTCLK is generated by an external clock generator. The NCR 7250 CRTC accepts Dot-Clocks up to 20 MHz. This Dot Clock provides the basic unit of timing for displaying information on the screen.

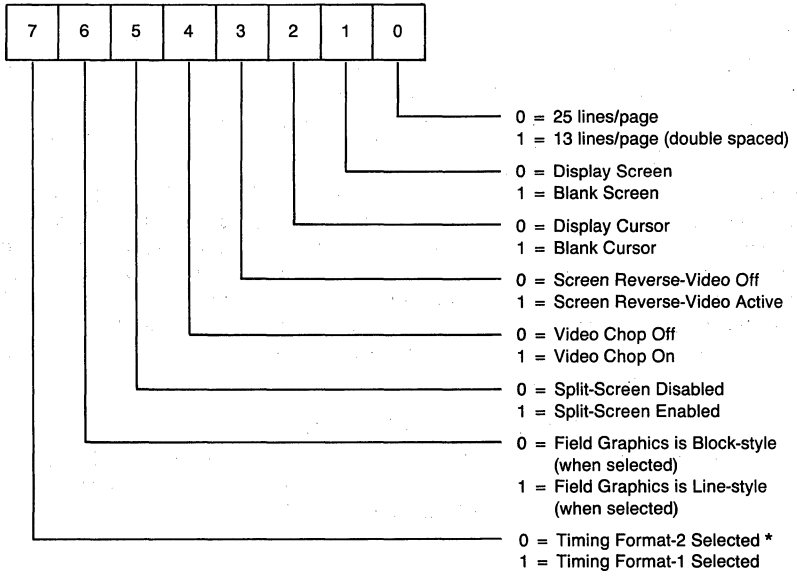
SOFTWARE FUNCTIONS

NCR 7250 CRTC software functions include eight Screen Functions and six Field Functions.

SCREEN FUNCTIONS

The Screen Functions available on the NCR 7250 CRTC are enabled/disabled by CPU command to the Special Functions Register (R4). Changes in R4 are not synchronized with video timing and appear on the screen at the time they are written.

SCREEN FUNCTION BIT ASSIGNMENTS



* The standard 7250 uses the Logic Level on pin 24 during RST to select the timing format. Timing format selection from the special functions register is available as a mask option.

FIELD FUNCTIONS

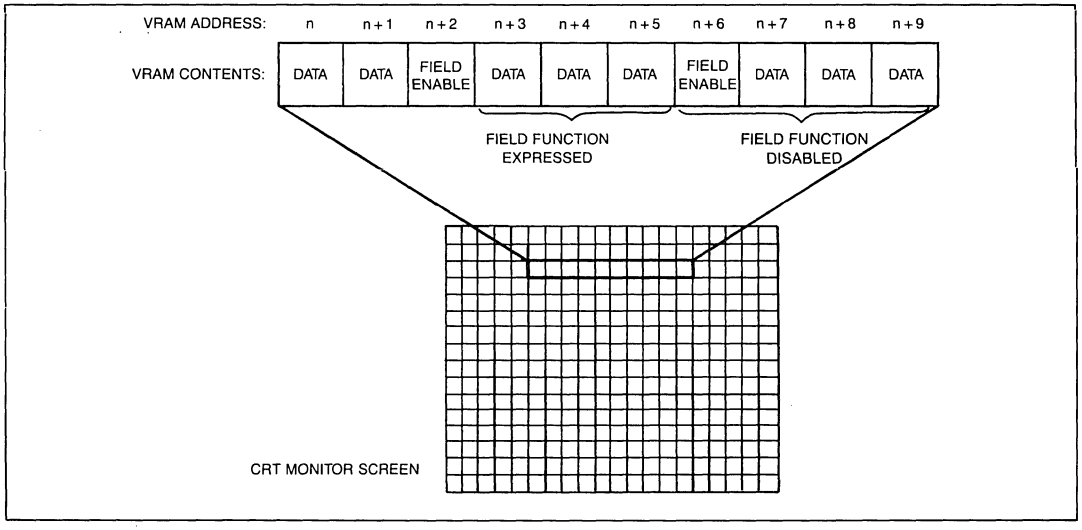
Field functions are selected by "control-bytes" which are loaded into VRAM along with display data. Bytes from VRAM are decoded by the character generator and by the field function control circuitry. Bytes having a value from 80H to BFH (bits 6 and 7 are 0 and 1 respectively) are detected as control bytes and provide the functions listed below. The corresponding location in the character ROM is coded as a blank. This permits the field function control words to be imbedded in the spaces normally occurring between words.

When a control byte is read in during the display process, the attributes selected are handled in three ways. For attributes which are deselected (a 0 in the the corresponding bit position), the attribute is turned off immediately and does not appear in the space occupied by the control byte. For attributes which are newly selected, the attribute will appear in the character position following the space occupied by the control byte. For attributes which were previously selected and again selected by the present control byte, that attribute will appear in a continuous manner, being displayed in the space occupied by the control byte.

FIELD FUNCTION BIT ASSIGNMENTS

Bit	Function
0	0 = Normal, No Reverse Video 1 = Reverse Video with Respect to Screen
1	0 = Normal, No Highlight 1 = Highlight Field with Respect to Screen Intensity
2	0 = Normal, Display Characters 1 = Initiate Field Blank
3	0 = Normal, No Blink 1 = Blink Character Field
4	0 = Normal, No Underline 1 = Underline All Characters within Field
5	0 = Bytes Interpreted as Characters 1 = Bytes Interpreted as Graphics-cells
6	Always 0
7	Always 1

FIELD FUNCTION ENABLED/EXPRESSED/DISABLED EXAMPLE



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GRAPHICS MODE FEATURES

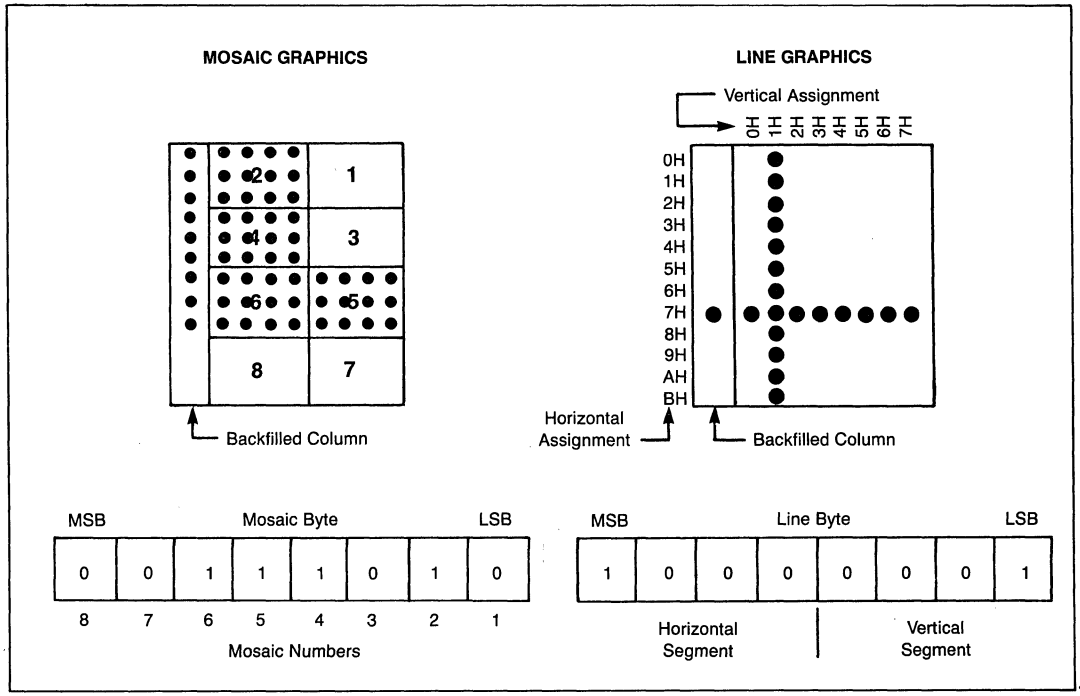
The Graphics capability of the CRTC is a special feature whereby the data bytes coming to the chip from VRAM cause the on-chip Character-ROM to send out special dot patterns. It allows the user to configure unique bar or line arrangements on the CRT monitor.

The Graphics Mode is selected by the Field Function logic. The user may choose one of two graphics styles: block or line. The graphics styles are selected via Bit 6 of the Special Functions Register.

When graphics mode is selected, the attributes selected at that time (blink etc.) are "latched-in" until the graphics mode deselect code is encountered. This permits the display of 255 different codes. The 256th code is reserved as the graphics mode deselect code and cannot be displayed. This code is mask programmable. The default value is C8H. The latching of functions affects only that graphics field. Other graphics field (with different latched attributes) and text with any combination of attributes can be displayed on the same screen.

In line graphics mode, single horizontal or vertical lines are produced by specifying a respective vertical or horizontal value which exceeds the values shown below. Spaces are produced by using values greater than C8H.

EXAMPLES OF BLOCK AND LINE GRAPHICS PATTERNS



MASK OPTIONS
(Available Upon Customer Request)

CHARACTER SET OPTIONS

FIELD FUNCTIONS AND CHARACTER SET SIZE

Because the inclusion of Field Functions means that the corresponding codes in the Character-ROM must be coded as blanks, there are less than 256 characters available to the user. There is a "trade-off" between the number of Field Functions and the size of the character set.

The standard NCR 7250 CRTC is equipped with all six Field Functions. If the user desires less than six functions (i.e., greater than 192 characters), mask options are available that may be changed accordingly.

FIELD FUNCTION/CHARACTER SET RELATIONSHIPS

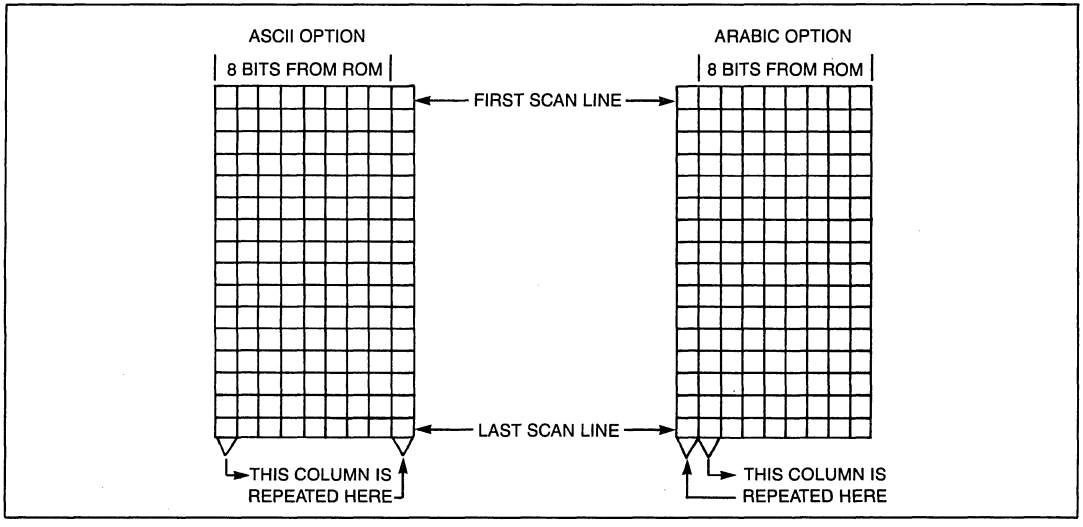
Number of Field Functions	Maximum Character Set Size
4	240
5	224
6	192

CUSTOMIZED CHARACTER SETS AND CHARACTER CODES

Character sets can be customized according to the user's requirements. Any coding for a new character set, however, should take account of the 9th dot derivations described below.

Backfilled Column—Character codes define eight horizontal dots per scan line of a character cell (usually as a hex-byte). The CRTC generates nine dots per scan line in driving the video display. The extra column of dots is derived from the first dot of each character scan line as shown in the following diagrams.

CHARACTER CODE OPTIONS



Note: Characters in a set are displayed under one of the above options only. The user must specify which option to use when a character set is customized.

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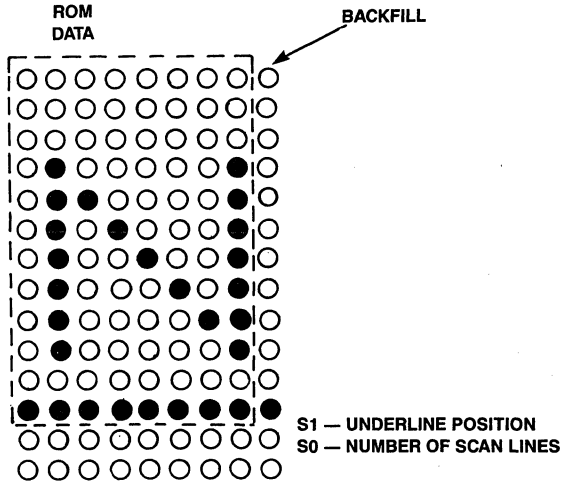
BLINK RATES

The number of frame-times counted in deriving the cursor and field blink rates is also a user-selectable option.

B0	Cursor	Field
1	12.50	3.12
2	6.25	1.56
3	4.17	1.04
4	3.12	0.781
5	2.50	0.625
6	2.08	0.521
7	1.79	0.446
8	1.88	0.469

CHARACTER CELL EXAMPLE

The size of the character cell can be selected by the user and masked into the NCR 7250 CRTC.



NOTE: The number of scan lines comprising a row of characters (16 lines maximum), and the position used for underline (any scan line) are mask programmable. The character generator produces an 8x12 block; backfill provides the 9th dot. In formats using more than 12 scan lines, the additional lines can be used for vertical spacing and underline.

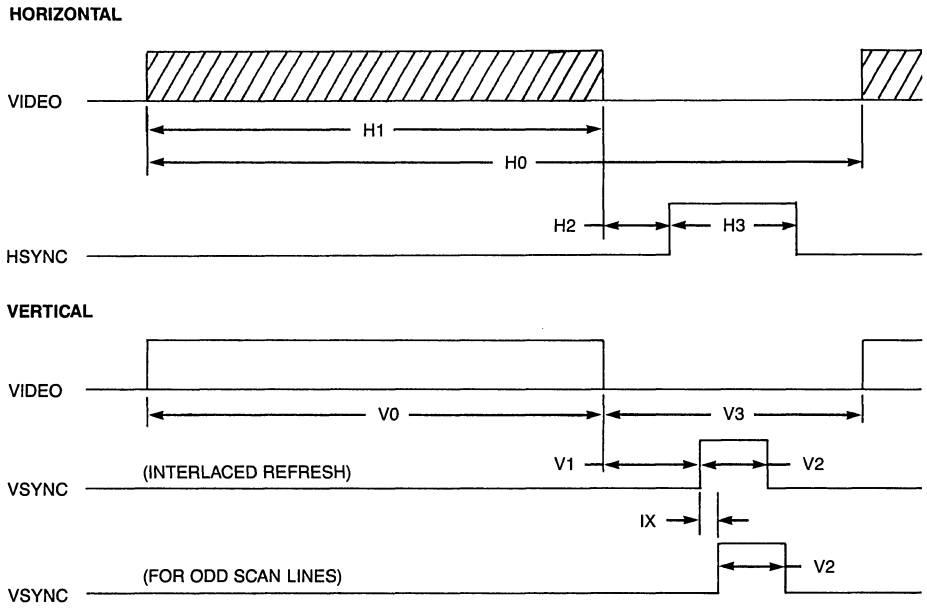
REGISTER OPTIONS

The address of the nine software display control registers are selected by the user and masked into the NCR 7250 CRTC.

GRAPHICS MODE DESELECT OPTION

The Graphics Mode Deselect Code default value may be changed from >C8 to a user-selected value.

MONITOR TIMING DIAGRAM



CRTC MONITOR TIMING

(Mask-Programmable: User selects two sets of the following parameters.)

Symbol	Parameter	Function
H0	Horizontal Scan-time	The duration in characters of a full horizontal period.
H1	Horizontal Character Count	The maximum number of characters that may appear on a displayed row of characters.
H2	Horizontal Front Porch	The delay in character-times between the last displayed row character-position, and the beginning of the HSYNC-pulse.
H3	Horizontal Sync-Width	The duration of the HSYNC-pulse in character-times.
V0	Vertical Row Count	The maximum number of displayed rows of characters.
V1	Vertical Front Porch	The delay in scan-times between the last character-position on the page, and the beginning of VSYNC.
V2	Vertical Sync-Width	The duration of the VSYNC-pulse in scan-times.
V3	Vertical Blank-Time	The duration of the VBLANK condition in scan-times.
S0	Character-Cell Height	The number of scan-lines used for each row of characters.
S1	Character Underline	The scan-line position of the Field Underline within the character cell.
B0	Basic Blink Rate	The number of frame-times counted in deriving the cursor and field blink rates.
IX	Interlace Offset	The number of character-times by which VSYNC (V1) is delayed on alternate frames, interlace modes.

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STANDARD MONITOR TIMINGS

Two timing formats are available in the Standard NCR 7250 CRTC Controller. Neither format is interlaced.

	60 Hz Format	50 Hz Format
H0	918 D[52 uS]	918 D[52 uS]
H1	720 D	720 D
H1	45 d	45 d
H3	81 D [4.6]	81 D [4.6]
V0	300 H	300 H
V1	63 D [.07 H]	29,430 D [32 H]
V2	2,745 D [2.99 H] [156]	3 H
V3	18,567 D [20.2 H] [1024]	77,317 D [84.2 H] [4,383]

NOTE: D = 1 Dot Clock
H = 1 Horizontal Scan Line Time (H0)
[ ] = Time in uS using 17.6 MHz Dot Clock

The following procedure is used to select either the 50 Hz or 60 Hz timing format:

1. Pulse the $\overline{RST}$ (pin 39) low for 10μs.
2. OE (pin 24) is held low to select 50 Hz.
   OE (pin 24) is held high to select 60 Hz.

It is recommended that a 33K ohm resistor be tied to 0 V or +5 V to select the desired timing format.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM STRESS RATINGS

Voltage on any pin with respect to ground (V_{SS}) . . . . . −.03 V to 7.0 V
Power Dissipation . . . . . 840 πW
Operating Temperature Range . . . . . 0°C to 70°C
Storage Temperature Range . . . −65°C to +150°C

The values listed here are absolute maximums which if exceeded could cause permanent damage to the device. All voltages are with respect to circuit ground.

ELECTRICAL CHARACTERISTICS

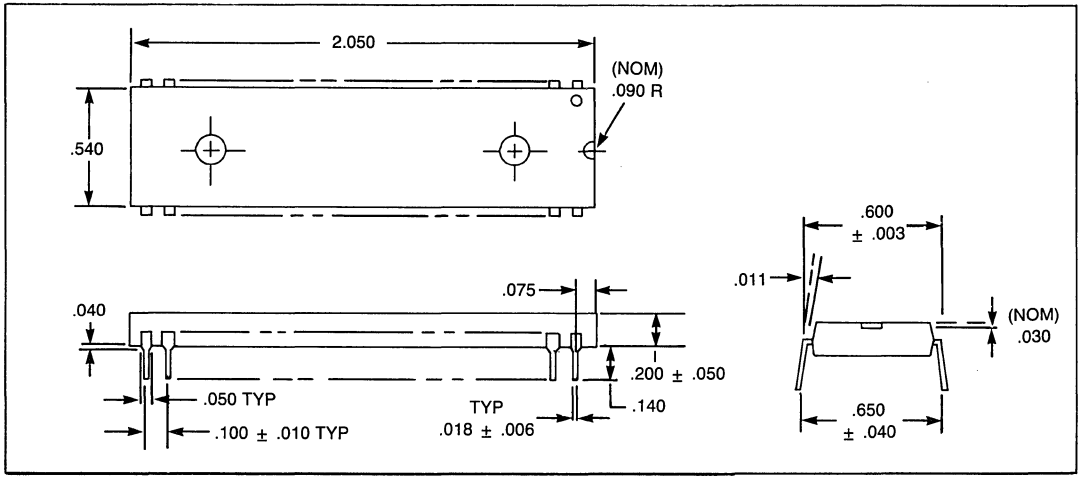
DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
V_{IL}	Input Voltage, Low	V_{SS}−0.3	0.8	V
V_{IH}	Input Voltage, High	2.0	V_{DD}	V
I_I	Input Leakage Current (V_{IN} = 0 to V_{DD})		±2.5	μA
V_{IL}CLK	Clock Input Voltage Low	V_{SS}-0.3	0.4	V
V_{IH}CLK	Clock Input Voltage High	2.4	V_{DD}	V
V_{OH}	Output Voltage, High (I_{OH} = −50μA)	2.7		V
V_{OL}	Output Voltage, Low (I_{OL} = 2 mA)		0.5	V
I_Z	Hi-Z Leakage Current (V_A = 0.4 to 2.4 V)	−10	+10	μA
I_{DD}	Power Supply Current (V_{DD} = 5.5 V)		120	mA

Note: All parameters shall be assured over the 0°C to 70°C temperature range and with $4.75 \leq V_{DD} \leq 5.25$V. Logic "1" is defined as the more positive voltage (V_{IH}, V_{OH}). Logic "0" is defined as the more negative voltage (V_{IL}, V_{OL}). All voltages are with respect to ground (V_{SS}).

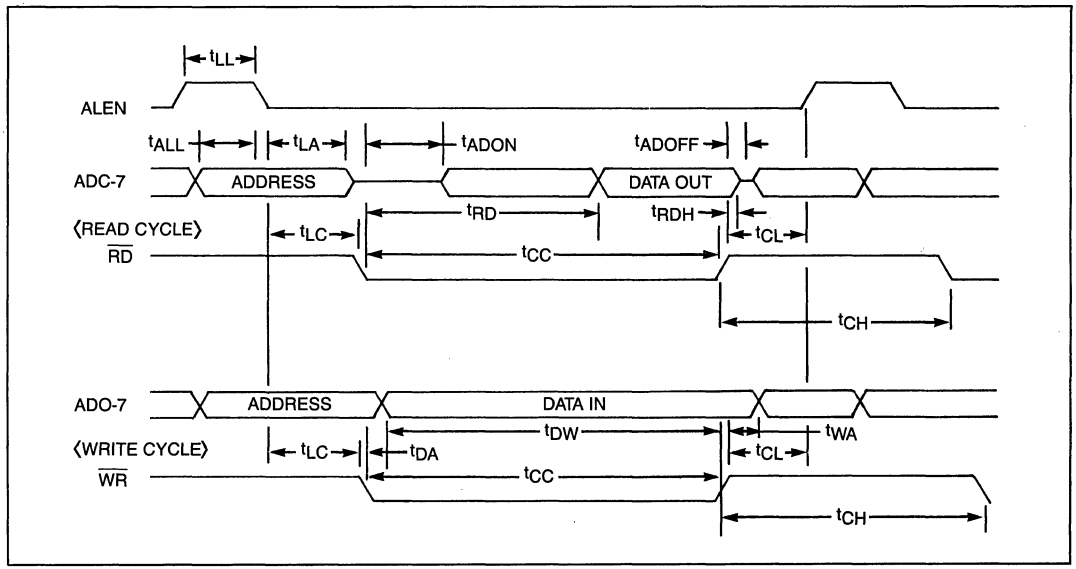
MECHANICAL DATA 40 PIN

PLASTIC DEVICES



MEMORY INTERFACE AND TIMING

PROCESSOR TIMING DIAGRAM



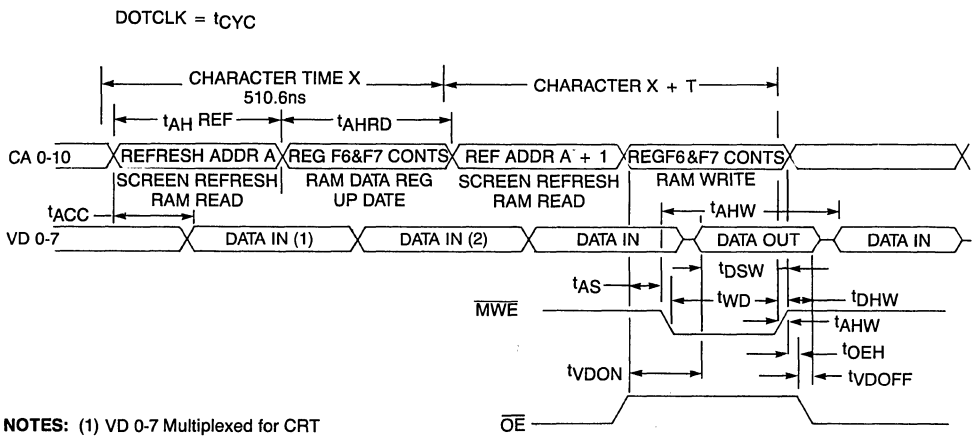
PROCESSOR BUS TIMINGS

Mnemonic	Parameter	Min	Max	Units
t_{LL}	ALEN Width	100		ns
t_{ALL}	Address Valid before ALEN	60		ns
t_{LA}	Address Hold after ALEN	60		ns
t_{LC}	ALEN to Control ($\overline{RD}$, $\overline{WR}$)	140		ns
t_{CC}	Control Width, ($\overline{RD}$, $\overline{WR}$)	350		ns
t_{RD}	Active RD to Valid Data		120	ns
t_{RDH}	Data Hold from $\overline{RD}$	0		ns
t_{CL}	Control ($\overline{RD}$, $\overline{WR}$) to ALEN	60		ns
t_{DW}	Data Valid Before $\overline{WR}$	300		ns
t_{WA}	Data Hold From $\overline{WR}$	55		ns
t_{DA}	Data Valid After $\overline{WR}$		100	ns
t_{ADON}	Address/Data Non-tri-state after $\overline{RD}$	50		ns
t_{ADOFF}	Address/Data tri-state	40	70	ns
t_{CH}	Time between active pulses	24 Dot Clocks - t_{CC}		ns

VRAM INTERFACE CHARACTERISTICS

In the VRAM timing diagram below, note that the second portion of a character-time is used to read VRAM data into the RAM-read register, unless a write command is issued. These CPU accesses (read or write) take place at the address contained in the Screen Address Register. No refresh VRAM accesses occur during blank times.

VRAM TIMING DIAGRAM



NOTES: (1) VD 0-7 Multiplexed for CRT
(2) VD 0-7 Multiplexed for F5 Data Register

Last portion of character time will always be used to continuously read data in the Video RAM into the RAM Data Register unless it is used as a write. The data read or write is at the RAM location specified in Address Register F6 and F7. Screen refresh RAM accesses do not occur during blank times.

VRAM INTERFACE TIMINGS

Symbol	Parameter	Min	Max	Units
t_{AHREF}	Valid Refresh Address Time	4(t_{CYC})	4(t_{CYC})	ns
t_{AHRD}	Valid Current Screen Address Time	5(t_{CYC})	5(t_{CYC})	ns
t_{ACC}	Valid Refresh Address to Valid Data In		150	ns
t_{AHW}	Current Screen Address Hold Time After $\overline{MWE}$	0		ns
t_{AS}	Current Screen Address Setup Time to $\overline{MWE}$	20		ns
t_{VDON}	Video Data Nontri-state from $\overline{OE}$	40		ns
t_{VDOFF}	Video Data Tri-State After $\overline{OE}$		5	ns
t_{DSW}	Valid Video Data Out Before $\overline{MWE}$	50		ns
t_{DHW}	Video Data Out Hold Time from $\overline{MWE}$	5		ns
t_{WD}	$\overline{MWE}$ Width	100		ns
t_{OEH}	OE Hold from $\overline{MWE}$	5		ns

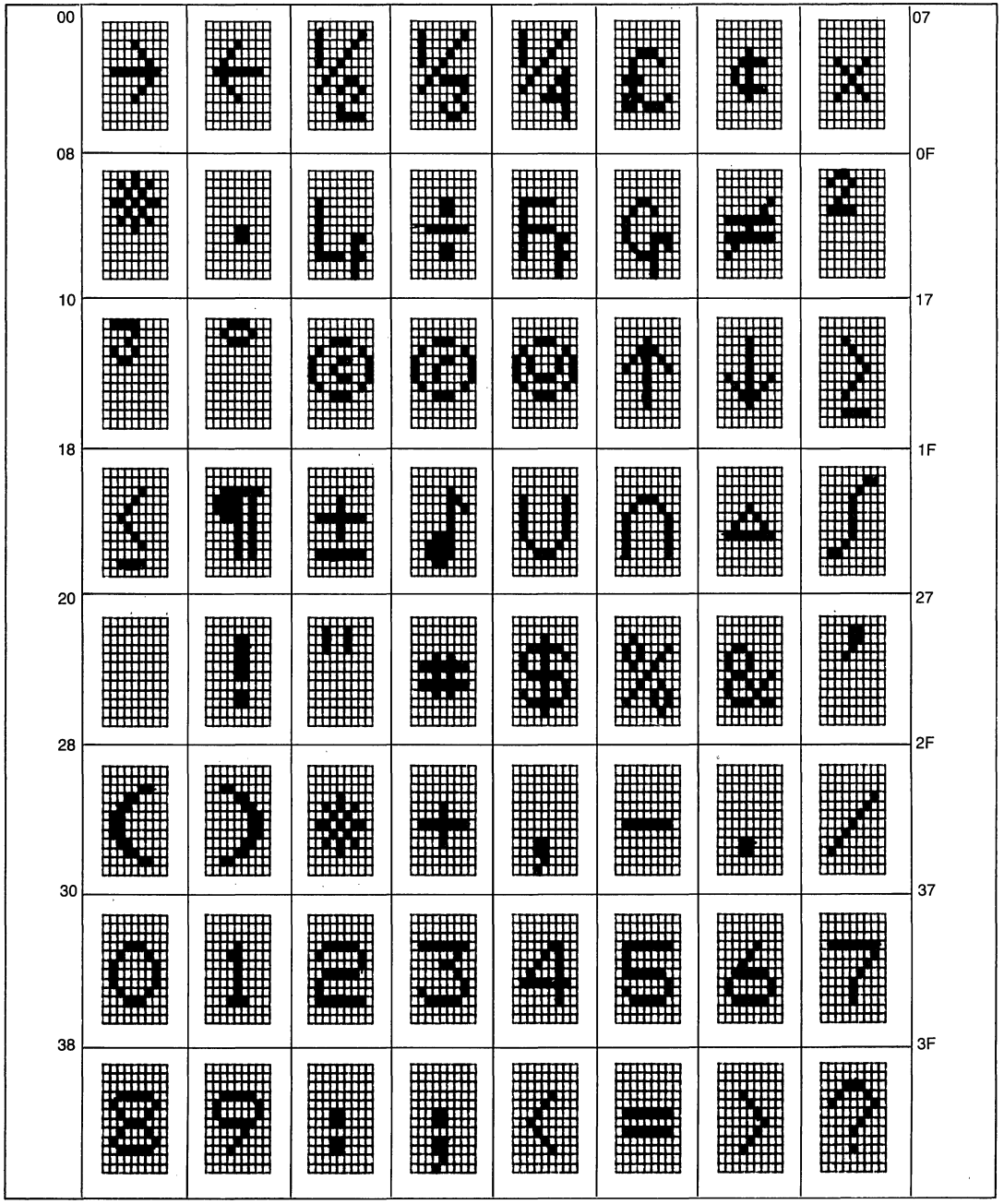
DOTCLK TIMINGS

Symbol	Parameter	Min	Max	Units
t_{CYC}	DOTCLK Period	50	75	ns
	DOTCLK Duty Cycle	45	55	%
t_{DKR}	DOTCLK Rise Time		10	ns
t_{DKF}	DOTCLK Fall Time		10	ns

NCR 7250 CRTC REGISTERS

Name	Address	Length	Function
Cursor Address	F0	11 Bits	Contains the VRAM Address of that character which exhibits the cursor.
Top of Page	F1	11 Bits	Contains the VRAM Address of that character which begins the page (i.e. top left corner).
Split Screen Address	F2	11 Bits	Contains the VRAM Address of the character that begins the designated split screen row.
Split Screen Row	F3	6 Bits	Contains the value of vertical counter at which the split screen address is first accessed.
Special Functions	F4	8 Bits	The bits of this register enable various attributes which affect the entire displayed screen.
Ram Write, Ram Read	F5	8 Bits	These two registers transfer bytes between the CPU and the VRAM. They are distinguished by pulsing either the $\overline{WR}$ or the $\overline{RD}$ pins.
Lower Screen Address	F6	8 Bits	This is the lower portion (stores LSB's) of the full Screen Address Register. It directly addresses the VRAM for CPU transfers.
Upper Screen Address	F7	3 Bits	This register contains the upper 3-bits of the Screen Address Register.

STANDARD CHARACTER SET



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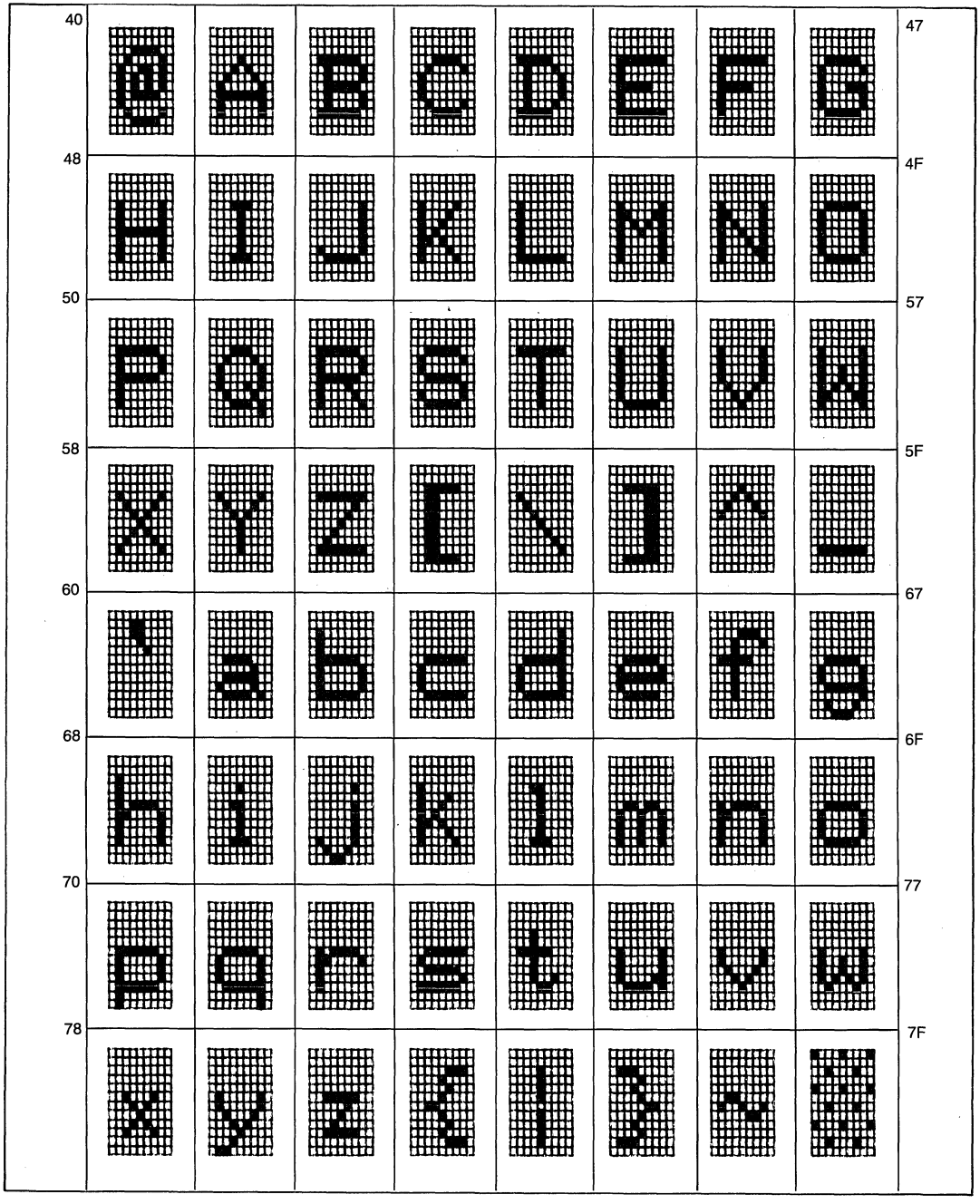
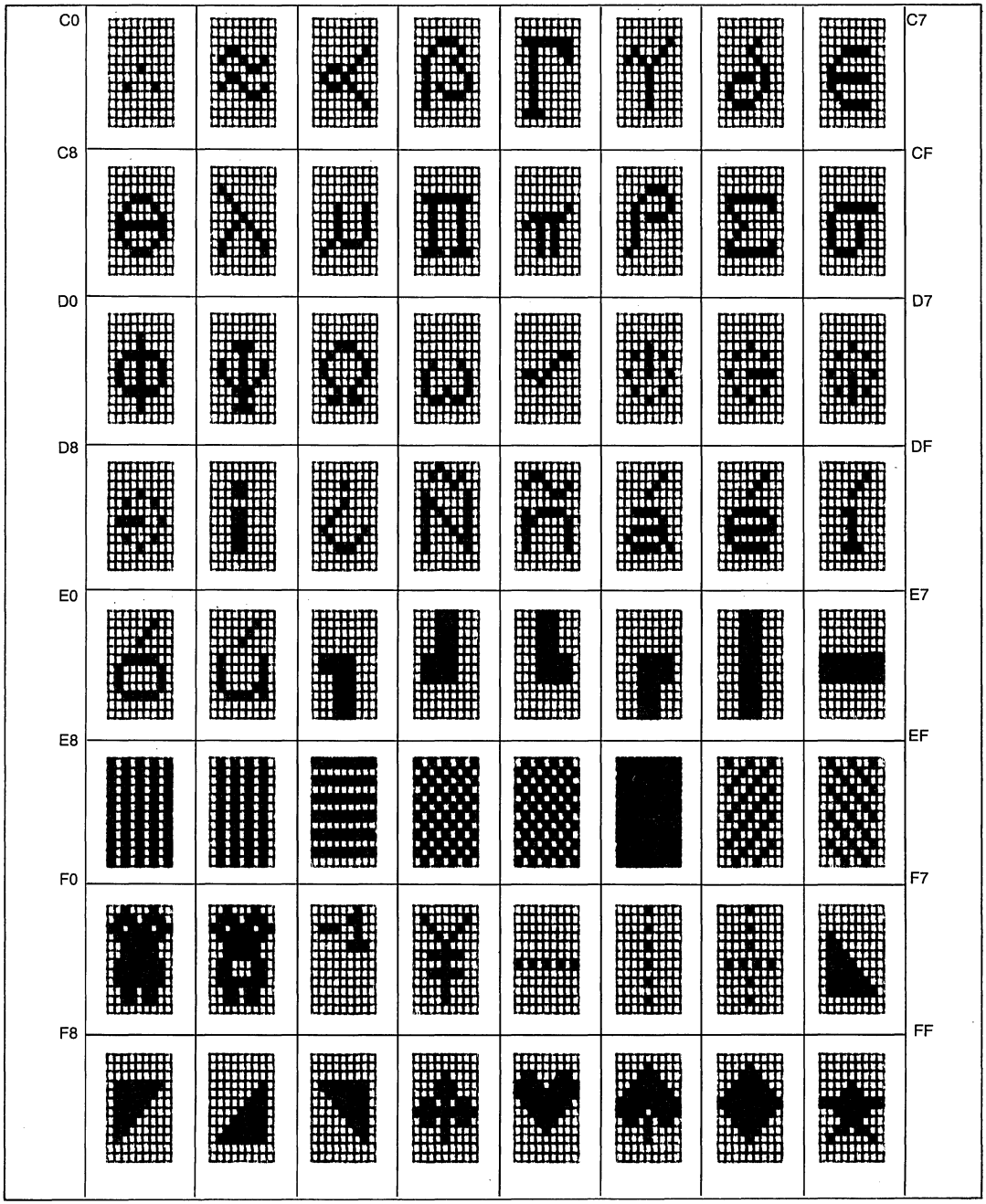
CHARACTER ADDRESS



CHARACTER ADDRESS



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